

**HD-line-camera VHDCAM02**

**Line-camera** with very high dynamic digital sensor and integrated processing unit

**Technical data:**

Pixelcount	:	128
Conversion	:	none, because a <b>digital sensor</b> <b>2 ... 20 Bit greyscale</b>
Exposure	:	automatically as function of maximal exposure defined exposure time <b>120dB global and local dynamic</b>
Trigger impulse	:	free running external, one line
Evaluation	:	control and processing by FPGA postprocessing and configuration per RISC- $\mu$ C
Outputs	:	RS232 via $\mu$ C 4 TTL-outputs , 3 TTL-inputs

The kernel of the **VHDCAM02** surmises a new digital linesensor with a high global dynamic. The sensor can working at a surrounding of 120dB brightness values, whereby he has locally a digital resolution of 20 bit.

Because the direct conversion from light in a digital number, this sensor is insensitive against disturbances. It has a full digital interface, which consist of address- and data bus. A random access to the pixels is possible.

The integration time for the sensor can be fixated pretend or limited by the Overflow of a Pixel. The control with Overflow optimized the sensor to the clearest pixel and scoops thereby always the complete possible dynamics.

With an resolution of 20 bit a Scanrate of 2 lines/s is reachable. With an reduction of resolution the speed of scanning become raised. So in a purely binary application the scanning rate of 100.000 lines/s with a resolution of 16 levels of grey can successes.

In order to handle the high data efficiency, the sensor in the camera is followed from free programmable logic (FPGA). This takes over the control of the Sensors and the evaluation of its incurring graphic data. It is qualified expressly for edge detection or widht measurement by quick processes. The FPGA has the possibility to send the results from the image processing directly to digital outputs.

To set parameter in the camera, an 8bit-RISC- $\mu$ C is inside, which communicate across a RS232-interface. It is possible to set modes and defined parameter for stand alone work in a EEPROM. He can also used for data aggregation at slow processes. The connection of user specific interfaces is possible.